

FIG. 1 is a block diagram of a radio system 100. The system 100 includes a host DSP 231, a RF/timing controller 233, a transmit controller/modulator 237, a RF transmit module 245, a duplexer 107, a 4x RF receiver module 205, an ADC 209, a down converter 213, and timeslot processors 217. The host DSP 231 is connected to the RF/timing controller 233, the transmit controller/modulator 237, and the duplexer 107. The RF/timing controller 233 is connected to the duplexer 107, the RF transmit module 245, and the 4x RF receiver module 205. The transmit controller/modulator 237 is connected to the RF transmit module 245. The RF transmit module 245 is connected to the duplexer 107. The 4x RF receiver module 205 is connected to the duplexer 107. The ADC 209 is connected to the 4x RF receiver module 205. The down converter 213 is connected to the ADC 209. The timeslot processors 217 are connected to the down converter 213. The duplexer 107 is connected to four antennas 103.

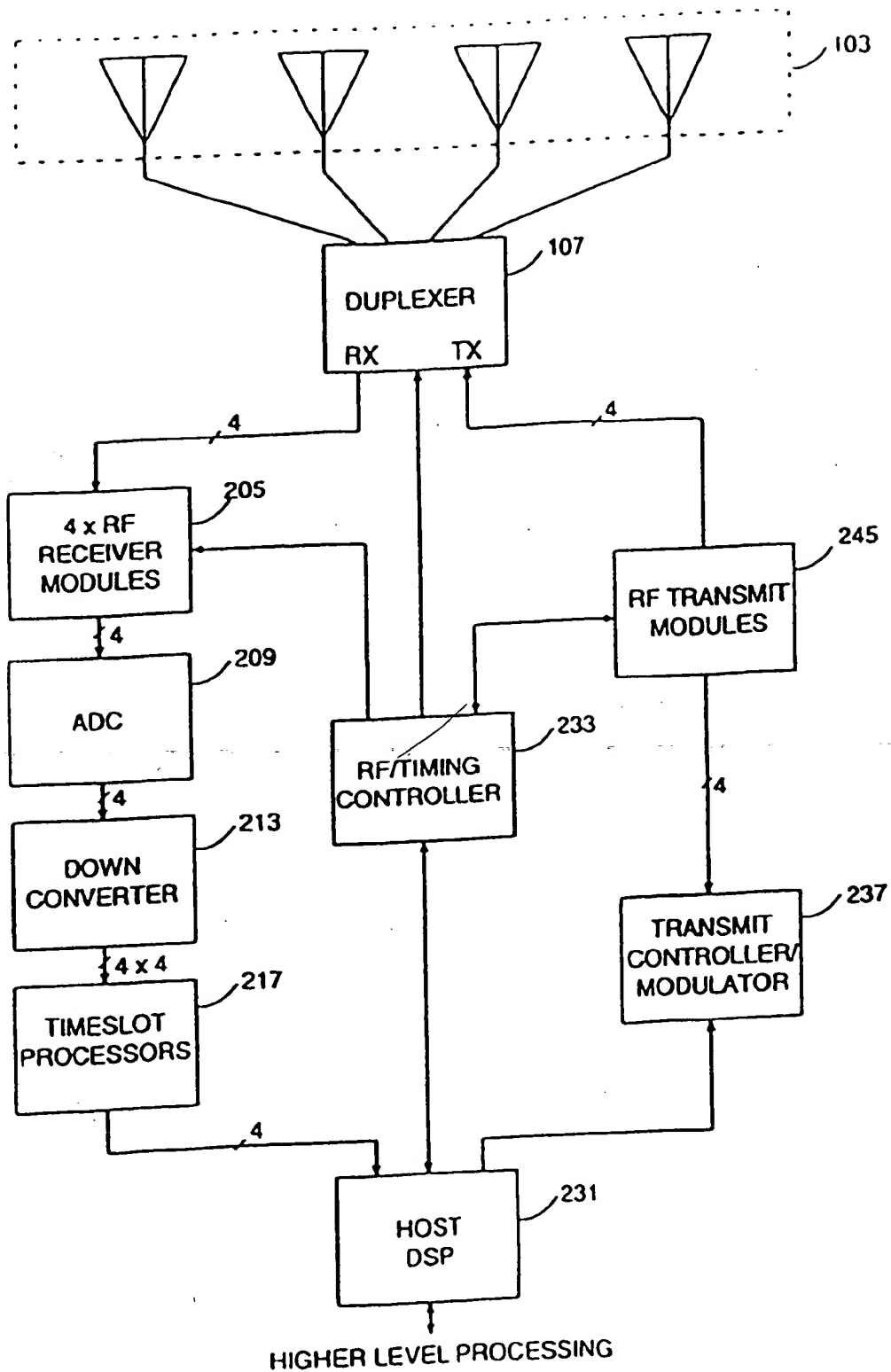


Figure 1

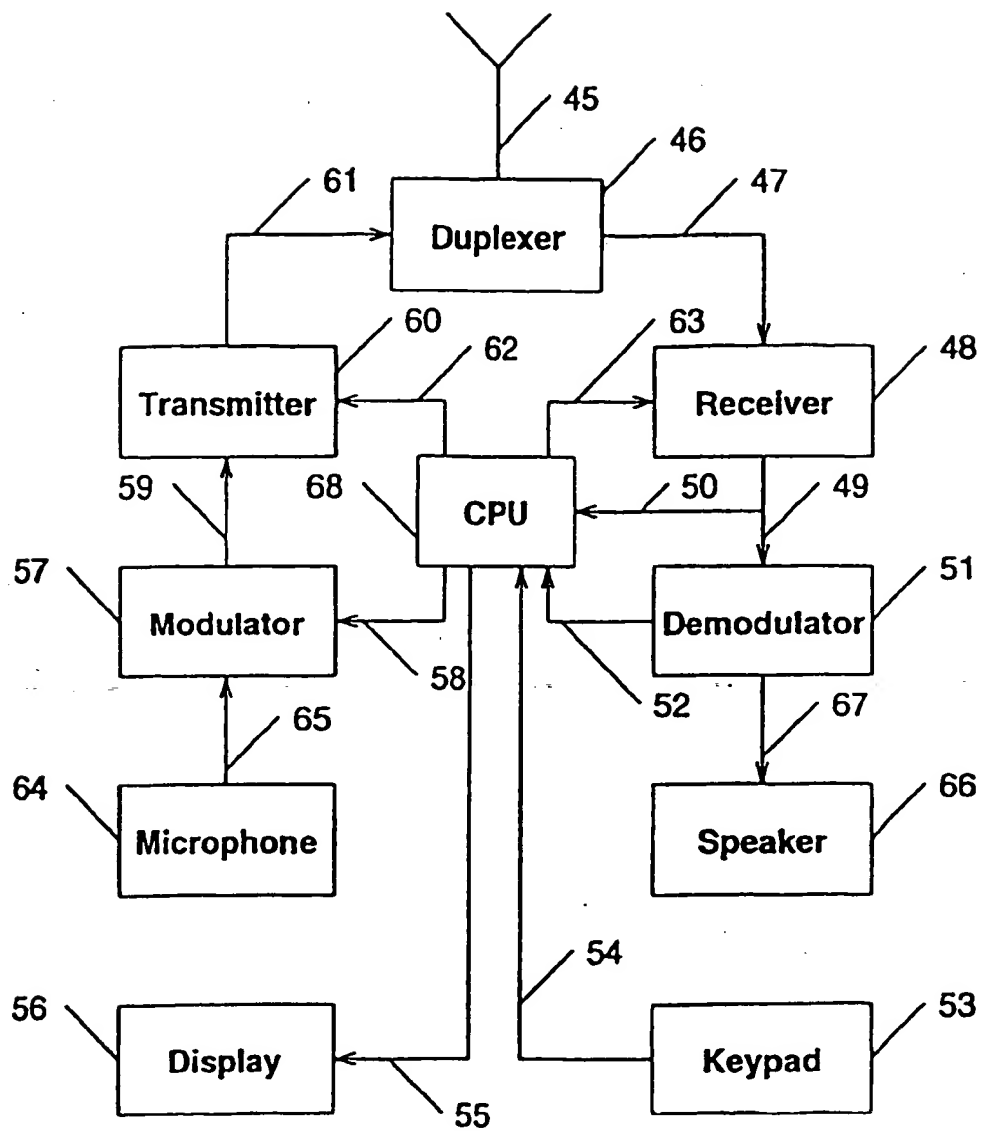


FIG. 2

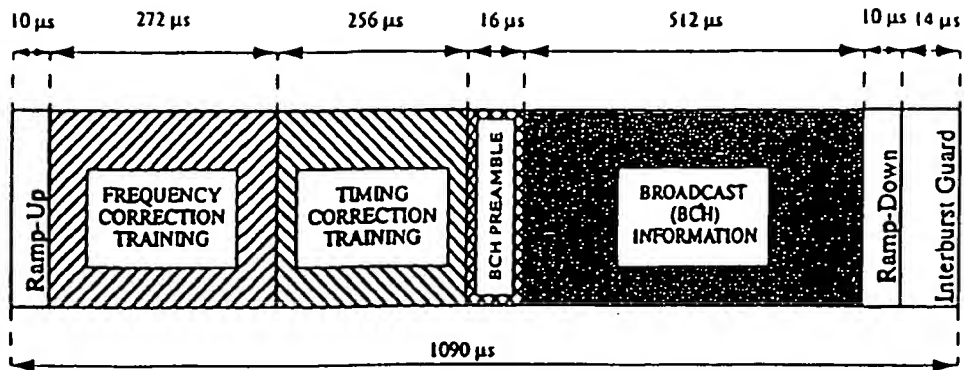


Fig. 3

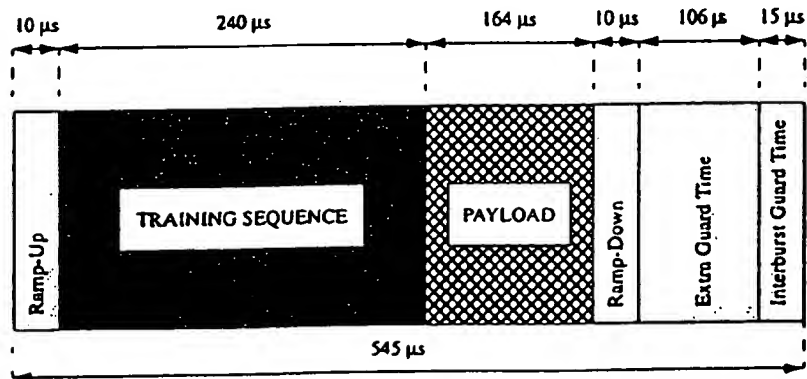


Fig. 4

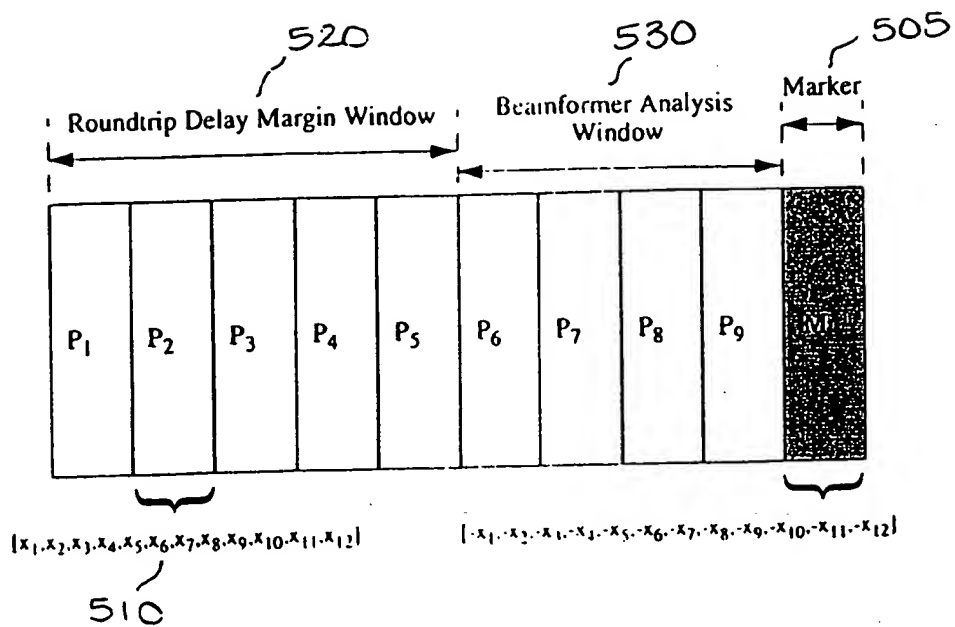


Fig. 5

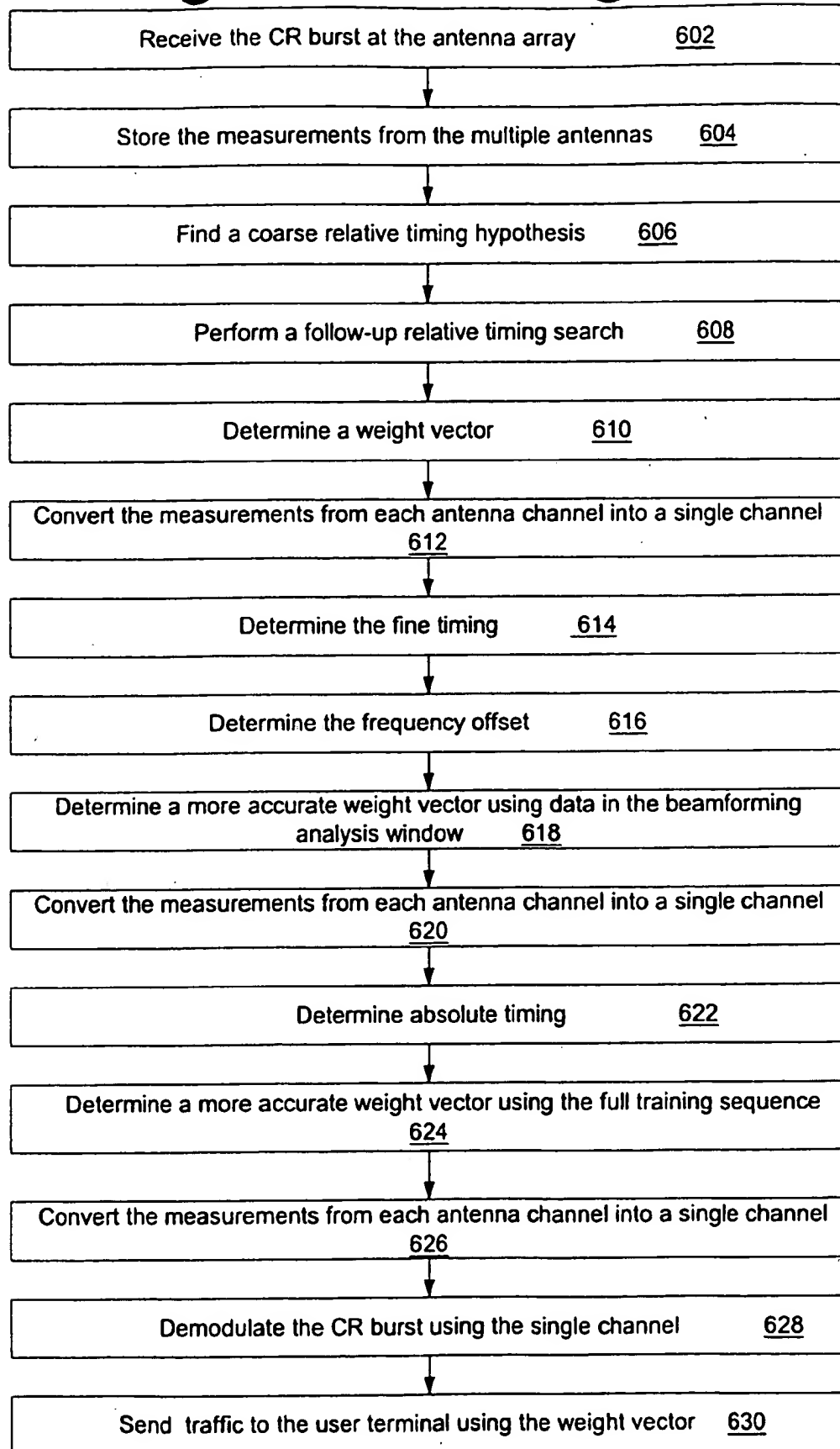


Figure 6

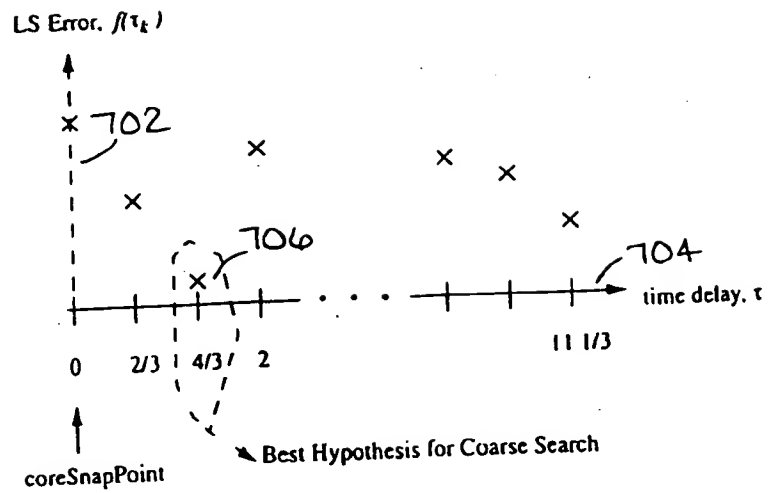


Fig. 7

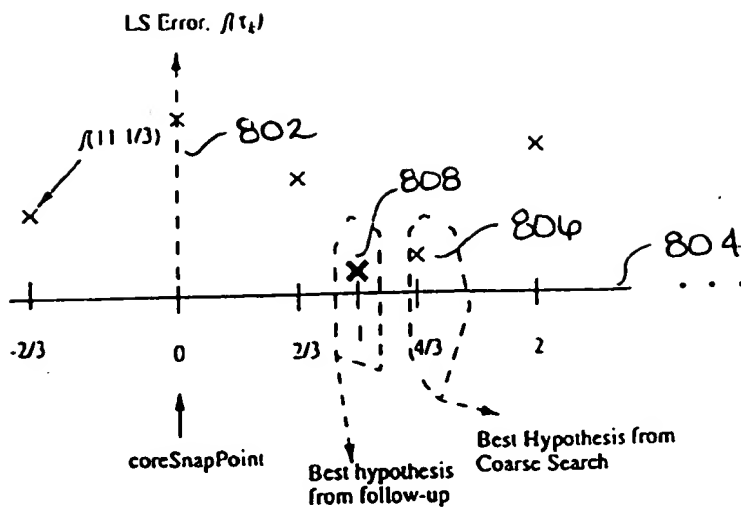


Fig. 8